TRANSMITTAL OF FORMAL DRAWINGS

Docket No.
BUR920040001US1 (17382)

In Re Application Of: John M. Cohn et al.

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/709,754	May 26, 2004	John P. Trimmings	23389	2117	3753

Invention: A SYSTEM AND METHOD OF PROVIDING ERROR DETECTION AND CORRECTION CAPABILITY IN AN INTEGRATED CIRCUIT USING REDUNDANT LOGIC CELLS OF AN EMBEDDED FPGA

Address to:
Commissioner for Patents
P.O. Box 1450
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Transmitted herewith are:

2 sheets of formal drawing(s) for this application.

☒ Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c).

Signature

Dated: February 15, 2008

Steven Fischman
Registration No. 34,594

SCULLY, SCOTT, MURPHY & PRESSER, P.C.
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